WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a regular cell array comprising regular memory cells;

a spare cell array comprising spare memory cells any of which is used in place of one of the regular memory cells when said one of the regular memory cells is defective;

first memory circuits each configured to store data indicating whether an associated one of the spare memory cells is used or not;

second memory circuits any of which is used to store address data indicating an address of said one of the regular memory cells which is defective;

a determining circuit configured to determine whether each of the spare memory cells is used or not, on the basis of data stored in an associated one of the first memory circuits;

a generating circuit configured to generate predetermined data; and

a selecting circuit configured to select and output one of the data generated by the generating circuit and address data stored in each of the second memory circuits.

2. The semiconductor integrated circuit according to claim 1, wherein the number of the second memory circuits is smaller than that of the spare memory cells

in the spare cell array.

3. The semiconductor integrated circuit according claim 1, wherein when a result of determination by the determining circuit indicates that said each spare memory cell is used, the selecting circuit selects the address data stored in an associated one of the second memory circuits, and when the result of determination by the determining circuit indicates that said each spare memory cell is not used, the selecting circuit selects the data generated by the generating circuit.

4. The semiconductor integrated circuit according to claim 1, which further comprises:

third memory circuits including shift registers and each configured to store the data output from the selecting circuit; and

an address determining circuit configured to compare the data stored in said each of the third memory circuits with address data input from an external device.

5. The semiconductor integrated circuit according to claim 1, which further comprises a counter configured to count the number of times the data is generated by the data generating circuit.

6. The semiconductor integrated circuit according to claim 1, which further comprises a clock controlling circuit configured to generate a clock signal for use in controlling timing of transferring each of the data

stored in said each first memory circuit and the data stored in said each second memory circuit.

7. The semiconductor integrated circuit according to claim 6, wherein the clock controlling circuit generates a clock signal for use in controlling a data shifting timing of the shift register of said each third memory circuit.

8. The semiconductor integrated circuit according to claim 1, wherein said each first memory circuit comprises a fuse element and a flip-flop configured to store data in accordance with whether the fuse element is cut or not, and said each second memory circuit comprises a plurality of fuse elements and a plurality of flip-flops configured to store data in accordance with whether the fuse elements are cut or not, respectively.

9. The semiconductor integrated circuit according to claim 8, wherein the flip-flop in said each first memory circuit and the plurality of flip-flops in said each second memory circuit are connected in series, thereby forming a shift register.

10. A method for transferring address data in a semiconductor integrated circuit comprising a spare cell array including spare memory cells any of which is used in place of one of regular memory cells in a regular cell array when said one of the regular memory cells is defective,

storing data indicating whether each of the spare memory cells is used or not, in an associated one of first memory circuits;

storing address data indicating an address of said one of the regular memory cells which is defective, in any of second memory circuits; and

determining whether said each spare memory cell is used or not, on the basis of the data stored in said associated one of the first memory cells, and then transferring, when determining that said each spare memory cell is used, address data which indicates an address of a defective one of the regular memory cells, and which is stored in an associated one of the second memory circuits, said defective one of the regular memory cells being replaced with said each spare cell, and transferring, when determining that said each spare memory cell is not used, the data generated by the generating circuit.

11. The method according to claim 10, which further comprises:

storing, in an associated one of third memory circuits, the address data indicating the address of said associated one of the regular memory cells and the data generated by the generating circuit; and

comparing the data stored in said associated one of the third circuits with address data input from an external device, and determining whether or not the

address indicated by the data stored in said associated one of the third memory circuits is the same as an address indicated by the address data input from the external device.

12. The method according to claim 10, wherein each of the first memory circuits comprises one fuse element, and each of the second memory circuits comprises a plurality of fuse elements.

13. The method according to claim 12, wherein:

said storing the data indicating whether said each spare memory cell is used or not, in said associated one of the first memory circuits, is achieved by cutting or not cutting the fuse element in said associated one of the first memory circuits; and

said storing address data indicting the address of said one of the regular memory cells which is defective, in said any of second memory circuits, is achieved by cutting or not cutting each of the plurality of fuse elements in said any second memory circuit.